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Package-on-Package (PoP), warpage, and Reliability

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Abstract
After a short overview of microelectronic packaging, the PoP – which allows vertically combining discrete logic and memory BGA packages – is presented. It allows multi-chip packages to be integrated for greater space savings on the printed circuit board (PCB). Instead of occupying multiple flat surface areas on the PCB, this allows the components to stack up much like a high-rise building. The paper is intended to inform the non-PoP technologists, researchers and decision makers about PoP reliability and some PoP actual problems.

Keywords: Microelectronic packaging, warpage, PoP reliability, PoP trends, 3D, SoC.

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