

Reliability Considerations at Nanometer Scale

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Abstract

This paper analyses some aspects concerning the reliability at nanometer scale. Although higher reliability is expected from submicron and nanotechnology so far only a few attempts have been made to apply reliability theory to submicron and nanodevices. The way to reliable nanotechnology is to identify relevant physical failure mechanisms and corresponding failure rates, determine reliability indices, and investigate reliability models down to nanoscale including quantum processes. Perhaps the most significant problem concerns the sensitivity of future IC generations face to various noise sources, and in particular face to energetic particles. This paper analyses some of the above problems. At the same time, we propose the implementation of a new soft error detecting technique based on time redundancy.

Keywords: Reliability, Fault tolerance, Redundancy, Submicron and nanodevices, Soft-error.

References:

- [1] M. Nicolaidis, Time Redundancy Based Soft-Error Tolerance to Rescue Nanometer Technologies, in Proceedings of the 17th IEEE VLSI Test Symposium, April 1999-07-12.
- [2] M. Alexandrescu, A Bacivarov, Tehnici de toleranță la defectări în circuitele CMOS submicronice, UPB, 2000.
- [3] U. Sennhauser, J. Reiner, P. Nellen, Nanoreliability, in Proceedings of 13th NID Workshop, 04-06 February 2004, Athens, Greece.
- [4] J.C. Reiner, P. Gasser, U. Sennhauser, Novel FIB- based sample preparation technique for TEM analysis of ultra thin gate oxide breakdown, in Microelectronics and Reliability, vol. 42, 2002.
- [5] S. Paul, C. Pearson, A. Molloy, M.A. Cousins, M. Green, S. Kolliopoulou, P. Dimitrakis, P. Normand, D. Tsoukalas M.C. Petty, Langmuir-Blodgett Film Deposition of Metallic Nanoparticles and their Application to Electronic Memory Structures, in Nano Letters, 3(4), 533-536 (2003).
- [6] M. Nicolaidis, N. Achouri, L. Anghel, Memory Built-In Self-Repair for Nanotechnologies, in IEEE International On-line testing Symposium, July 2003, Kos, Greece.
- [7] M. Nicolaidis, N. Achouri, L. Anghel, A Memory Built-In Self-Repair for High Defect Densities Based on Error Polarities, in IEEE Defect and Fault Tolerance Symposium, November 3-5, 2003 – Cambridge, MA, U.S.A.
- [8] M. Nicolaidis, N. Achouri, L. Anghel, A Diversified Memory Built In Self Repair Approach for Nanotechnologies, in IEEE VLSI Test Symposium, April-May 2004, Napa Valley, CA, USA.
- [9] D. Alexandrescu, L. Anghel, M. Nicolaidis, New Methods for Evaluating the Impact of Single Event Transients in VDSM Ics, in Proceedings of the 17th IEEE International Symposium on Defect and Fault-Tolerance in VLSI Systems, 6-8 November 2002, Vancouver, Canada.
- [10] C. Roman, S., Mir B. Charlot, Building an analogue fault simulation tool and its application to MEMS, in Microelectronics Journal, Vol. 34, No.10 , 897-906 , 2003.