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Test, Testability and Reliability Aspects of Integrated Circuits

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Abstract

The role of testing is to detect whether something went wrong and the role of diagnosis is to determine exactly what went wrong. Testability is a design criterion and should be included in design reviews. Quiescent power supply current (IDDQ) testing of a CMOS integrated circuit is a technique for production quality and reliability improvement, design validation, and failure analysis. It has been used for many years by a few companies and has now receiving wider acceptance as an industry tool.

Keywords: ASIC, IDDQ, NNR, SEC, TCV, operational test, test methods, reliability

References:

- [1] IEEE, IEEE STD 1522-2004 Trial-Use Standard for Testability and Diagnosability Characteristics and Metrics, Jan. 2004.
- [2] Department of Defense, MIL-STD, 2165 Military Standard Testability Program for Electronic Systems and Equipments, Washington, DC, January 26, 1985.
- [3] Testability.com, The Information Source for System Testability and Diagnostic, http://www.testability.com/Reference/Glossaries.aspx?Glossary=Testability.
- [4] High Performance Analog Solutions, Lexicon of Semiconductor Terms, http://rel.intersil.com/docs/lexicon/T.html.
- [5] K.-T. Cheng, et al., "A Partial Scan Method for Sequential Circuits with Feedback," IEEE Trans. on Computers, Vol. 39, 1990, No. 4, pp.544-548.
- [6] R. Gupta, et al., "The BALLAST Methodology for Structured Partial Scan Design," IEEE Trans. on Computers, Vol. 39, No. 4, 1990, pp.538–543.
- [7] Y. Bo, et al., "Testability Design for Sequential Circuit with Multiple Feedback," Proc. The fourth Internat. Conf. on Solid–State and Integrated–Circuit Technology, Beijing, China, Oct. 24-28, 1995, pp.208-210.
- [8] J. M. Soden, et al., "IDDQ Testing: A Review," A Special Issue of Journal of Electronic Testing; Theory and Applications (JETTA), No.3, 1992, pp. 291-303.
- [9] R. K. Gulati, and Ch. F. Hawkins (Eds.), "IDDQ Testing of VLSI Circuits." A Special Issue of Journal of Electronic Testing; Theory and Applications (JETTA), Vol. 3, No. 4, 1993.
- [10] R. Rajsuman, IDDQ Testing for CMOS VLSI, Norwood, MA, Artech House, 1994.
- [11] R. Rajsuman, "IDDQ Testing for CMOS VLSI". Proceedings of the IEEE. 88 (4)2000, 544–568.
- [12] W. R. Daasch, et al, Neighborhood Selection for IDDQ Outlier Screening at Wafer Sort, http://doi.ieeecomputersociety.org/10.1109/MDT.2002.1033795
- [13] W. Riordan, et al., "Microprocessor Reliability Performance as a Function of Die Location for a 0.25 μ , Five Layer Metal CMOS Logic Process," Reliability Physics Symposium Proceedings, 1999, 37th Annual IEEE International Symposium, 1999, pp. 1-11.

Asigurarea Calitatii - Quality Assurance, ISSN 1224-5410 Vol. XXIV, Issue 96, October-December 2021 Pages 16-21

- [14] P. D. T. O'Connor, Practical Reliability Engineering, Chichester, New York, J. Wiley, 2002.
- [15] T. I. Băjenescu, Reliability of Electronic Components, Bucharest, Tehnica Publishing House, 1996.
- [16] T. I. Băjenescu and M. I. Bâzu, Component Reliability for Electronic Systems, Artech House, Boston & London, 2010.
- [17] S. Kayali, G. Ponchak, R. Shaw, "GaAs MMIC Reliability Assurance Guideline for Space Applications," Chapter 7, https://parts.jpl.nasa.gov/mmic/7.PDF
- [18] S. Hamdioui, "VLSI Test Technology and Reliability," https://www.researchgate.net/file.PostFileLoader.html?id..., 2010.
- [19] IEC 61000-4-30: Testing and Measurement Techniques.
- [20] H. Vermaaak, Design-for-Delay-Testability. Techniques For High-Speed Digital Circuits, Ph. D. Thesis, Universiteit Twente, 2005.
- [21] J. M. da Silva, "Test and Design for Testability of Analog and Mixed-Signal Circuits," 2010, https://indico.cern.ch/event/78641/attachments/1058996/1510087/TDfTAMS-part1.pdf